How to Trade Leakage for Tamper-Resilience

Daniele Venturi

Joint work with: Sebastian Faust (Katholieke Universiteit Leuven) Krzysztof Pietrzak (CWI Amsterdam)



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Tamper-Proof Circuits

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1 Define model & security notion

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• This is done through a security game involving some





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2 Build cryptoscheme



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 - Often a too strong statement, as it e.g. implies $\mathbf{P}\neq\mathbf{NP}$ $\textcircled{\sc or}$



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- - 3 Formally prove security: Show that no (efficient) adversary can win the security game
 - Often a too strong statement, as it e.g. implies $\mathbf{P} \neq \mathbf{NP}$ \odot
 - We can prove conditional result ©

Security proof implies:



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• Security against all known and future attacks



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- Security against all known and future attacks
- Can we go home and relax?





- Security against all known and future attacks
- Can we go home and relax?
- Provably secure systems get broken in practice!



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secret state



Cryptosystem

• Security proofs usually rely on the black-box model





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 - has only black-box access to the cryptosystem
 - $\bullet\,$ he can specify an input X
 - $\bullet\,$ and gets the corresponding output Y
 - the computations within the box stay secret

public parameters



secret state





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- Passive [•] can apply side-channel attacks: e.g. measuring time, sound, heat while the crypto-device is working
 - This results in a leakage Λ about the secret state. Even partial leakage suffices to break the cryptosystem [Kocher96]



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- Active value of the apply tampering attacks: e.g. expose it to UV radiation, heating up the device
 - The modified output can completely expose the secrets stored in the device [BDL00]





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A general question

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Consider any Boolean circuit C.



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- \bullet C can be randomized



A general question

Question:

Consider any Boolean circuit C. Is it possible to formally prove that C is secure against an (as large as possible) class of fault attacks?

- C is a directed acyclic graph:
 vertices ⇔ gates, edges ⇔ wires
- C can be stateful: input X_i and memory M_i are used to produce output Y_i and new state M_{i+1}
- C can be randomized



Compilers

A possible solution using the notion of circuit compiler:



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• Transform C in another circuit \widehat{C} , in such a way that tampering in \widehat{C} is detected with high probability
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• Φ is functionality preserving: C with initial state M_0 and \widehat{C} with initial state \widehat{M}_0 result in an identical output distribution

• Consider a computationally unbounded (∞, δ) -adversary tampering adaptively with \widehat{C} for many rounds



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Tamper-Proof Circuits

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- Finally we gets the output of \widehat{C} when tampering is applied to the computation

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[IPSW06]

(t, 0)-tamper resilience of [IPSW06]





Apply up to t faults



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 - Requires $O(k^2)$ bits of fresh randomness per invocation



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Our paradigm: trading leakage for efficiency



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- Our paradigm: trading leakage for efficiency
- Obscription of our compiler



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- Our paradigm: trading leakage for efficiency
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- Onclusions and perspective

$(\infty, \delta, \overline{\lambda})$ -tamper resilience





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$(\infty, \delta, \overline{\lambda})$ -tamper resilience





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Apply unbounded # faults



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Tamper-Proof Circuits

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$(\infty, \delta, \lambda)$ -tamper resilience



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Tamper-Proof Circuits

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Our result

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 - Positive results from leakage-resilient cryptography



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Simulation is hard because



Our Compiler



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- Idea: Guarantee that \widehat{C} outputs
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 - Constant 0 if tampering occurs (we can reply with 0)
- Avoid: Tampering successfully without being noticed



Big picture of \widehat{C} (k = 3)



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• The core of \widehat{C} consists of k sub-circuits (same topology as C)



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- A wire $w \in \{0,1\} \Rightarrow \operatorname{MMC}(w) = (w \oplus r, r, \overline{w} \oplus r', r')$
- NAND \Rightarrow NAND (see below)


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- Valid output of core: k copies of MMC(w), ∀w ∈ output of C (2k bits of randomness in total)



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Computes with MMC





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MMC(w NAND w')

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MMC(w)



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• Invalid inputs generate 0^4

• Assumed tamper-proof



MMC(w)

MMC(w')





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Say output is 0, i.e. all wires are 0
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Say output is 0, i.e. all wires are 0 and wants to change it to 1
Just set every wire to 1: Prob. of success increases with # of wires!





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- Just set every wire to 1: Prob. of success increases with # of wires!
- MMC prevents this attack: error will propagate!
- Composition lemma: Tampering in a sub-circuit ⇒ output of core will contain invalid encoding w.h.p.



• So changing the output of core will fail, but ^{we} can tamper over many rounds!





- So changing the output of core will fail, but 😻 can tamper over many rounds!
- Cascade phase will avoid this



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 - Invalid input ⇒ output will encode 0: self-destruct mechanism



- So changing the output of core will fail, but 🦋 can tamper over many rounds!
- Cascade phase will avoid this
 - Invalid input \Rightarrow output will encode 0: self-destruct mechanism
 - Tamper-proof gadgets of linear size (but same for every circuit)

 $\bullet\,$ We don't know how to prove without them $\odot\,$



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• Tampering with the input induces some distribution



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- Tampering with the input induces some distribution
- The deeper we go the "worse" this distribution can be made

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- Tampering with the input induces some distribution
- The deeper we go the "worse" this distribution can be made
- Open question: find a construction for the NAND such that the bias cannot be increased





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tampers with \widehat{C} the following can happen

O Tampering changes encoding of w to encoding of 1 - w



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 \clubsuit tampers with \widehat{C} the following can happen

- **(**) Tampering changes encoding of w to encoding of 1 w
 - Cannot be simulated
 - We show it happens with negligible probability
- No tampering: use black box access for simulation
- Tampering detected: output 0









• However does not know when this will happen

• Give as advice $\Lambda = f(M_0)$ the exact point of failure





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• Give as advice $\Lambda = f(M_0)$ the exact point of failure

In which invocation



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- Give as advice $\Lambda = f(M_0)$ the exact point of failure
 - In which invocation
 - At which point of the cascade phase



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• Finally, simulation must continue even after self-destruct





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• Give as advice $\Lambda=f(M_0)$ the exact point of failure

bits

In which invocation

• At which point of the cascade phase

- Finally, simulation must continue even after self-destruct
 - Looks trivial since the state is destroyed, but recall that faults are persistent

Take-home message

It is possible to compile any circuit such that it resists an unbounded number of faults



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- **2** Trading a small amount of leakage can lead to efficient compilers



Conclusions

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- **2** Trading a small amount of leakage can lead to efficient compilers
 - Where do we go from here?

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 - Eliminate tamper-proof gadgets

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- **2** Trading a small amount of leakage can lead to efficient compilers
 - Where do we go from here?
 - Dependent errors
 - Global tampering functions
 - Eliminate tamper-proof gadgets
 - Implementation-independent model

Questions?

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